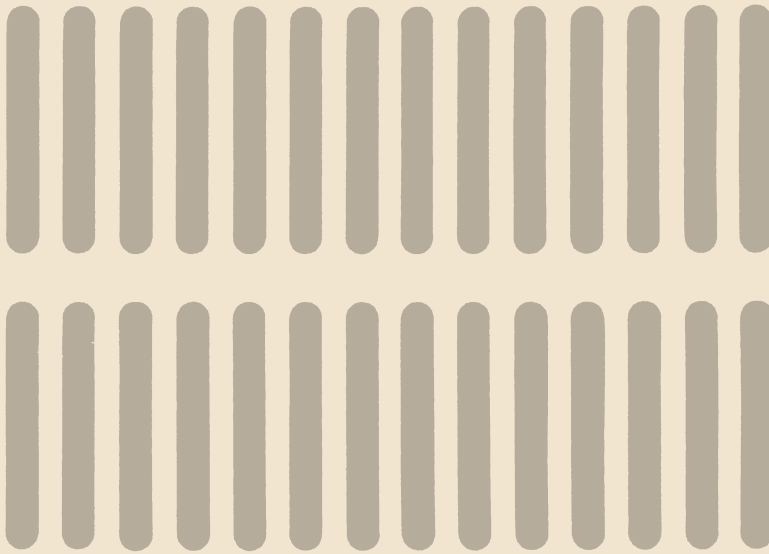
VAX11/750

Self Maintenance Diagnostic Guide



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EK-750YA-UG-001

VAX11/750

Self Maintenance Diagnostic Guide

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FIGURES

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HOW TO USE THIS GUIDE

This guide contains information needed for diagnosing VAX-11/750 hardware problems. It does not tell how to solve these problems, but does save looking through larger books for key items you usually want to know.

First, scan the Table of Contents to find what areas are covered. Second, take this guide with you when diagnosing the VAX-11/750. Unless you memorize the contents, this guide is the easiest way to carry information needed to fix a computer problem.

> NOTE
> **The term DM in this guide refers to the diagnostic module option on the VAX-11/750. The designation for this option is KC750-YA. Ignore the parts of this guide that refer to the DM if your system is not equipped with the KC750-YA option.**

VAX-11/750 SYSTEM OPERATING STATES

State	Description
Program I/O	This is normal operating state of VAX-11/750. CPU is running under stored program control.
VAX console	CPU is under control of its own console microcode. CPU console commands are supported in this state. Console prompt (>>>) is displayed by terminal.
DM console control mode	This is the same as program I/O state if CPU is running except CTRL/D changes system to DM console state command mode; running program supplies terminal prompt. If CPU is halted, it is the same as VAX console state where VAX console prompt (>>>) is displayed.
DM console command mode	System recognizes DM commands only. DM> prompt is displayed.
Micro-diagnostic	DM is under control of micro-diagnostic monitor (MICMON). MIC> prompt is displayed.

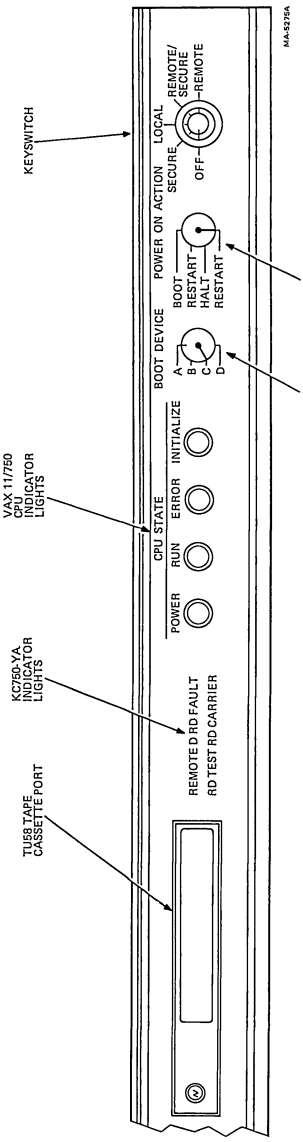

Figure 1 VAX-11/750 Front Panel

VAX-11/750 KEYSWITCH POSITIONS

Position	Description
LOCAL SECURE	System only responds to local terminal. Program I/O state is enforced.
LOCAL	System only responds to local terminal. System responds to CTRL/D and CTRL/P to change state.
REMOTE SECURE	Same as LOCAL SECURE
REMOTE	Same as LOCAL

VAX-11/750 PANEL LIGHT INDICATORS

Indicator	Description
POWER	Console is supplied with proper voltage. (VAX-11/750 processor can lose partial power and still light the LED and allow diagnostic tests.)
REMOTE D	Not used
REMOTE	Not used
RD Fault	DM logic has failed. Fault LED should light for about 10 seconds during console power-up as part of logic self-test.
Run	Program is running in CPU.
RD TEST	Not used
ERROR	When blinking, this indicates control store parity error. When on, it indicates double control store parity error and CPU clock has stopped.
RD CARRIER	Not used

DM COMMAND SET

Command	Syntax	Function
Clear	CL	Clear stop-on-micromatch
Deposit	D [/ modifier] [address] ⟨data⟩	Deposit to VAX memory location

DM COMMAND SET (Cont)

Command	Syntax	Function
Examine	E [/ modifier] [address]	Examine VAX memory location
Examine-Console	E/C [address]	Examine DM status registers
Initialize	INI	Initialize
Link	LIN	Enter link control file
Load	LO ⟨file name.ext⟩ [address]	Load TU58 file to VAX memory
Micro-address	UA ⟨address⟩	Load CS address bus
Micro-address/C	UA/C ⟨address⟩	Load CS address bus until next M clock only
Parity	PAR ⟨address⟩	Run control store parity check
Perform	PER	Perform link control files
Repeat-Last-Command	REP	Repeat console command
Repeat-Next-Command	R ⟨command⟩	Repeat following command
Return	RET	Return to program I/O state
Return/D	RET/D	Return to DM control mode

DM COMMAND SET (Cont)

Command	Syntax	Function
Set	SE [address]	Set stop-on-micromatch
Show	SH	Show CPU state
Show-Version	SH/V	Show current version of DM firmware
Step	STE	Step through single micro-instruction
Step-Tick	STE/T	Step through single clock tick
Stop	STO	Stop clock
Test	TE	Load and run micro-diagnostics
Test-Com	TE/C	Load micro-monitor and await command
Test-File	TE ⟨file name.ext⟩	Load and run user DM program
Trace	TR	Display trace of CS address.

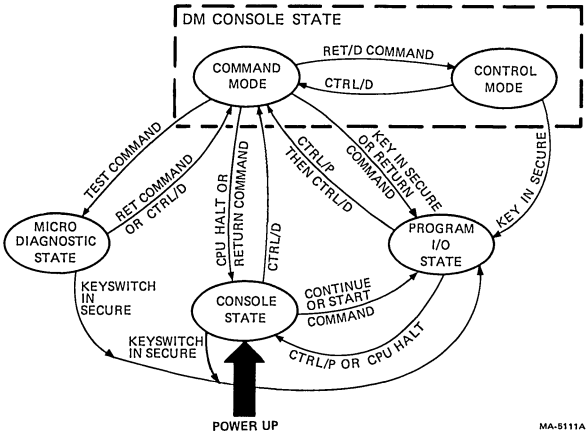

Figure 2 DM Operating State Transitions

DM ERROR MESSAGE CODES

Code	Definition
TAP:14	Tape – read length ERROR, not all records fit
TAP:13	Tape – flag received, not command or data
TAP:12	Tape – directory error
DM:11	Invalid operation code in macro
DM:10	Operation already in progress
TRM:0D	Terminal – length of input longer than buffer
TRM:0B	Terminal – command input buffer overloaded
TAP:09	Tape – file not found
TAP:08	Tape – invalid packet received
TAP:07	Tape – no end packet, invalid operation code received
TAP:06	Tape – tape count byte received exceeds maximum
TAP:05	Tape – tape checksum error received

DM ERROR MESSAGE CODES (Cont)

Code	Definition
	NOTE **UARTs are DM resident.**
TAP:04	Tape UART – received overflow
TAP:03	Tape UART – data set ready dropped
TAP:02	Tape UART – error received from UART
TAP:01	Tape UART – device timed out
CPU:04	CPU UART – received overflow
CPU:03	CPU UART – data set ready dropped
CPU:02	CPU UART – error received from UART
CPU:01	CPU UART – device timed out
TRM:04	Terminal UART – received overflow
TRM:03	Terminal UART – data set ready dropped
TRM:02	Terminal UART – error received from UART
TRM:01	Terminal UART – device timed out
TAP:FF	Tape – diagnostic failure
TAP:EE	Tape – partial operation (end of medium)
TAP:F8	Tape – bad unit number
TAP:F7	Tape – no cartridge
TAP:F5	Tape – write protocol
TAP:EF	Tape – data check error
TAP:EO	Tape – see error (block not found)
TAP:DF	Tape – motor stopped
TAP:DO	Tape – bad operation code
TAP:C9	Tape – bad record number
SYNTAX ERROR	Error in entering console commands

DM ERROR MESSAGE CODES (Cont)

Code	Definition
INVALID COMMAND	DM does not recognize command
CMI:nn	Error in VAX main memory (two digits, nn, are error code) Results from EXAMINE if area addressed has error
CMI:00	Nonexistent memory
CMI:01	Corrected read data
CMI:02	Read data substitute
ROM	ROM failed DM power-up selftest
RAM	RAM failed DM power-up selftest

MICMON COMMANDS (DM equipped systems only)
The following commands are listed in alphabetical order. Enter only the capitalized characters. Arguments in angle brackets are mandatory. Arguments in square brackets are optional. Do not type the brackets. When arguments are shown separated by a slash line, you must type one of the arguments, but not both.

CLear CF: ⟨dcs-address⟩ ⟨bit-number⟩
Clears specified ⟨bit-number⟩ in control file of ⟨dcs-address⟩.

CLear FLag ⟨flag-name-list⟩
Clears (disables) specified program control flag.

CLear SOmm: [cs-address]
Clears stop-on micromatch function. To create a scope sync pulse at a specified DCS address add 1800 to the desired DCS address. If cs-address is specified, a scope sync pulse is generated on backplane slot 6 pin C81 when the current address matches cs-address. Pulse occurs with M clock at beginning of the specified CS-address.

COntinue
Continues execution of program, following error detection or CTRL/C.

DIagnose QV
DIagnose PAss: ⟨pass-count⟩
DIagnose TEst: ⟨test-number⟩ [test-number/COntinue]
Diagnose command initializes program control flags and starts execution of a test program.

LOop
Puts program into error loop after it detects and reports an error.

REturn
Returns VAX-11/750 from MICMON to DM command mode.

SEt CF: ⟨dcs-address⟩ ⟨bit-number⟩
Sets specified ⟨bit-number⟩ in control file of specified ⟨dcs-address⟩.

SEt FLag ⟨flag-name-list⟩
This command sets (enables) any program control flag.

SEt SOmm: ⟨cs-address⟩
Stops execution of code in DCS at a specified DCS address.

SEt STep CYcle
Steps through DCS microinstructions one CPU machine cycle (M clock) at a time.

SEt STep INstruction [:test-pc]
Steps through pseudo instructions in current test. If test-pc specified, step function will not start until instruction at test-pc is ready to be executed. If test-pc not specified, stepping begins at next pseudo instruction of current test following a Loop or Continue command.

SEt STep TIck
Steps through DCS microinstructions one B clock at a time.

SHow FLags
Displays current states of program control flags.

SHow VBus
Displays current signal states on visibility bus.

MICMON FLAGS

Flag	Description
HALT	Halt – Call the monitor when an error is detected and the error message has been typed.
LOOP	Loop on error – Only useful for program-detected error. It is set by LOOP command. It can also be set manually by typing SE FL LO. When it is set and program detects an error, test loops on minimum amount of code necessary to recreate error. However, when set manually, you must clear the HALT flag and set the NER flag if program is to loop on error continuously without error reports.

MICMON FLAGS (Cont)

Flag	Description
LOOP (Cont)	The loop executed may include pseudo instructions and DCS microinstructions, running from the ERRLOOP instruction to the IFERROR instruction in the failing test. Or the loop may include DCS microinstructions only. If the IB flag is set, or if a microinstruction trap occurs, the program will not loop on the microinstructions in DCS. Error messages are not inhibited while the loop is executing unless the NER flag is set. Type CTRL/C to escape from the loop and return to monitor.
NER	No error report – If this flag is set, program does not report errors.
BELL	Bell on error – If this flag is set, program rings terminal bell on first occurrence of an error and on every fifth occurrence.
SA	Signature analysis – If this flag is set, program loops on test in progress, between BEGINSA and ENDSA pseudo instructions. Loop occurs whether test detects errors or not. Set SA flag when signature analyzer is used to help diagnose faults. This flag provides two sync points on backplane: a start/stop window (slot 6, pin C75); and a clock pulse (slot 6, pin C73). With test looping and signature analyzer connected to sync points, signature analyzer analyzes any test point that the probe samples. Signature analyzer displays a value (signature) if signal pattern is steady. Compare this value with corresponding value from a known good module to locate failures.
QA	Quality assurance – When this flag and the LOOP flag are set, the program will not try to loop on DCS microcode only. Instead, it will loop between the ERLOOP and IFERROR pseudo instructions.
IB	Inhibit burst flag – When this flag and the LOOP flag are set, the program will not attempt to loop only on DCS microcode. Rather, it will loop between ERRLOOP and IFERROR pseudo instructions.
TR	Trace flag – When this flag is set, monitor prints test names as well as numbers.

VAX CONSOLE COMMANDS

Command	Function
CTRL/P	Enter VAX console state
CTRL/D	Enter DM console state
E [/ modifier] [address]	Examine
D [/ modifier] [address] ⟨data⟩	Deposit
I	Initialize processor and UNIBUS
T	Test VAX by running microverify
S	Start program in CPU
C	Continue microcode execution at address in PC
N	Single step CPU through macroinstruction (after PC is loaded)
B	Boot CPU from device selected by front panel device switch
X	APT load and dump

COMMAND MODIFIERS FOR EXAMINE AND DEPOSIT COMMANDS

DATA TYPE

Modifier	Data Type
/B	Byte
/W	Word
/L	Longword

COMMAND MODIFIERS FOR EXAMINE AND DEPOSIT COMMANDS (Cont)

ADDRESS SPACE

Modifier	Address Space
/G	GPR
/I	IPR
/P	Physical memory
/V	Virtual memory
⟨space⟩P	PSL

NOTE
When you type CTRL/P while system is already in VAX console state, system responds with)))/ prompt.

COMMAND SWITCHES FOR BOOT COMMAND

Switch	Function
/X	Boot device selected by front panel switch; microverify inhibited.
/ nnnn	Boot device selected by front panel switch; 4-digit argument becomes boot control flags for VMB.EXE in R5.
⟨space⟩ ⟨device⟩	Boot device specified by operator

BOOT CONTROL FLAGS

Flag	Function
0	Conversational boot – Causes the system to ask for various kinds of information during the boot procedure.
1	Debug – Causes the Executive Debugger to be included in the VMS running system.
2	Initial breakpoint – If this flag and the flag bit 1 flag are set, causes a breakpoint to occur right after the Executive enables mapping.
4	Diagnostic boot – Causes a boot by filename for the Diagnostic Supervisor.
5	Bootstrap breakpoint – Causes the bootstrap to stop at breakpoints in VMB and SYSBoot.

BOOT CONTROL FLAGS (Cont)

Flag	Function
6	Image header – Causes the transfer address from the image header of the boot file to be used. Otherwise, control goes to the first byte of the boot file.
7	Memory test inhibit – Causes the bootstrap to ask for the name of the boot file.
8	File name – Causes the bootstrap to ask for the name of the boot file.
9	Halt before instruction – Causes a system halt prior to transfer of control to the secondary boot file.

EXAMPLES OF VAX CONSOLE COMMANDS

Example	Explanation
⟩⟩⟩	Console prompt
⟩⟩⟩D/G/L F 1000⟨CR⟩	Put 1000H in PC
⟩⟩⟩D/P 1000 005251D0⟨CR⟩	Put code in address 1000H
⟩⟩⟩E/I 25⟨CR⟩	Examine cache disable register
⟩⟩⟩I⟨CR⟩	Initialize CPU
⟩⟩⟩B/10/X DMA0⟨CR⟩	BOOT diagnostic supervisor without microverify from DMA0

CONSOLE COMMAND ERROR CODES

Code	Description
20	Deposit or Examine of memory failed. (This could mean one of following has occurred: access violation; translation not valid; bus error; TB parity error; control store parity error.)
11	Illegal access of an IPR
30	APT loading checksum error
33	Attempt to boot from unknown device type (DM, DL, DT, DR)
34	Boot device controller not A, B, C, or D.

EXAMPLE OF CONSOLE COMMAND ERROR

Example	Description
))) E P⟨CR⟩	Examine PSL
))) E⟨CR⟩	Illegal attempt to examine next address
?11	Illegal access of IPR
)))	System ready for new command

CONSOLE HALT ERROR CODES

Code	Description
01	Execute TEST console
02	CTRL/P halt or single macro instruction mode
04	Interrupt stack not valid
05	Microverify test failure
06	Halt instruction executed
07	Vector bits ⟨1:0⟩ = 3, halt at vector
08	Vector bits ⟨1:0⟩ = 2, WCS disabled or not present
0A	Change mode instruction executed on interrupt stack
0B	Change mode instruction executed and vector ⟨1:0⟩ not = 0
11	Power up and can't find RPB, FPS1 at RESTART/HALT
12	Power up and warm start flag false FPS1 at RESTART/HALT
13	Power up and can't find good 64K of memory
14	Power up and booting, but bad or no Boot ROM
15	Power up and cold start flag set during boot subroutine
16	Power up halt FPS1 at HALT position

CONSOLE HALT ERROR FORMAT

When the system enters the console state on a halt, it prints out the PC and a 2-digit console halt error code.

Format	Description
00010003 06 〉〉〉	Indicates halt instruction executed at address 10003.

POWER-UP TERMINAL DISPLAY FORMATS

Display	Description
%% 00000000 16 〉〉〉	Power-up with power-on action switch set to HALT. System passes power-on self-tests.
%F 00000nnn FF	Power-up with power-on action switch set to HALT. F indicates failure of M temp scratch pad test. Three-digit hexadecimal number is current PC+2 and points to failing test. (See microverify codes.) FF indicates microverify failure.
%%%% nnnnnnnn 13 〉〉〉	Power-up with power-on action switch in RESTART/BOOT or BOOT. Indicates a good 64 Kb section of memory was not found and system returns to console mode. Eight-digit code is PC+2 and loop count.
%%%% nnnnnnnn 14 〉〉〉	Power-up with power-on action switch in RESTART/BOOT or BOOT. Indicates a failed or missing boot ROM. Eight-digit code is PC+2 and loop count.
nnnnnnnn 06 〉〉〉	Occurs on execution of a Halt instruction after typing a console boot command. Indicates a failure of the read of logical block 0 of the selected boot device. Eight-digit code is PC+2 and should equal base address of first good 64 Kb of memory plus FX16 for TU58 or FX20 for RX06. This failure occurs in the BOOT ROM routine.

MICROVERIFY CODES

Code	PC+2	Test Name/Error Message
'@'		RBUS, WBUS TEST
	000	BAD BIT IN DREG OR SUPROT
	001	BAD BIT IN RBUS OR WBUS
'C'		MBUS TEST
	031	BAD BIT IN QREG
	033	BAD BIT IN MBUS
'E'		SCRATCH PAD BIT TEST
	051	ERROR CLEARING RTEMP
	052	ERROR FILLING RTEMP WITH ONES
	054	ERROR CLEARING GPR
	057	ERROR FILLING GPR WITH ONES
	058	ERROR CLEARING IPR
	05B	ERROR FILLING IPR WITH ONES
	05D	ERROR CLEARING MTEMP
	05E	ERROR FILLING MTEMP WITH ONES
'F'		MTEMP EXPLICIT ADDRESS TEST
	061	ERROR ADDRESSING MTEMP0
	062	ERROR ADDRESSING MTEMP1
	064	ERROR ADDRESSING MTEMP2
	067	ERROR ADDRESSING MTEMP4
	068	ERROR ADDRESSING MTEMP8
'I'		RTEMP EXPLICIT ADDRESS TEST
	091	ERROR ADDRESSING RTEMP0
	092	ERROR ADDRESSING RTEMP1
	094	ERROR ADDRESSING RTEMP2
	097	ERROR ADDRESSING RTEMP4
	098	ERROR ADDRESSING RTEMP8
'J'		IPR EXPLICIT ADDRESS TEST
	0A1	ERROR ADDRESSING IPR0
	0A2	ERROR ADDRESSING IPR1
	0A4	ERROR ADDRESSING IPR2
	0A7	ERROR ADDRESSING IPR4
	0A8	ERROR ADDRESSING IPR8
'L'		GPR EXPLICIT ADDRESS TEST
	0C1	ERROR ADDRESSING R0
	0C2	ERROR ADDRESSING R1
	0C4	ERROR ADDRESSING R2
	0C7	ERROR ADDRESSING R4
	0C8	ERROR ADDRESSING R8
	0CE	ERROR ADDRESSING DUAL PORT

MICROVERIFY CODES (Cont)

Code	PC+2	Test Name/Error Message
'O'		XB/IR/OSR BIT TEST
	0F1	ERROR IN XB31:0⟩
	0F2	ERROR IN XB63:32⟩
	0F4	ERROR IN IR
	0F7	ERROR IN OSR
'Q'		SOURCE XB PC INCREMENT TEST
	111	ERROR SOURCING ONE BYTE FROM XB
	112	ERROR SOURCING 2 BYTES FROM XB OR INCREMENTING PC BY 1
	114	ERROR SOURCING AN UNALIGNED LONGWORD OR INC PC BY 2
	117	ERROR INCREMENTING PC BY 4
'R'		RNUM/DSIZE TEST
	121	ERROR READING DSIZE ROM OPERAND 1
	122	ERROR LOADING/READING RNUM
	124	ERROR READING DSIZE ROM OPERAND 2
	127	ERROR LOADING/READING RNUM
	128	ERROR READING DSIZE ROM OPERAND 3
	12B	ERROR LOADING/READING RNUM
	12D	ERROR READING DSIZE ROM OPERAND 4
	12E	ERROR LOADING/READING RNUM
'T'		RNUM/DSIZE TEST CONTINUED
	141	ERROR READING DSIZE ROM OPERAND 5
	142	ERROR LOADING/READING RNUM
	144	ERROR READING DSIZE ROM OPERAND 6
'X'		CACHE PARITY ERROR TEST
	181	FAILED TO GET CACHE PARITY ERROR
	182	BAD MACHINE CHECK ERROR SUMMARY REGISTER
	184	BAD CACHE ERROR REGISTER
'['		TB PARITY ERROR TEST
	1B1	FAILED TO GET GROUP 0 TB PARITY ERROR

MICROVERIFY CODES (Cont)

Code	PC+2	Test Name/Error Message
'[' (Cont)	1B2	BAD TB GROUP PARITY ERROR REGISTER
	1B4	BAD MACHINE CHECK ERROR SUMMARY REGISTER
	1B7	FAILED TO GET GROUP 1 TB PARITY ERROR
	1B8	BAD TB GROUP PARITY ERROR REGISTER
	1BB	BAD MACHINE CHECK ERROR SUMMARY REGISTER
']'		CONTROL STORE PARITY ERROR TEST
	1D1	FAILED TO GET CONTROL STORE PARITY ERROR
	1D2	ERROR IN CONTROL STORE PARITY ERROR
'•'		CACHE TEST
	1E1	ERROR FILLING CACHE WITH ONES. LOCATION NOT INITIALLY = 0
	1E2	ERROR FILLING CACHE WITH ONES. UNABLE TO WRITE ONES

VMB PRIMARY BOOT FAILURE CODES

Code	Description
%BOOT-F-Unknown Processor	Indicates CPU is not a VAX-11/750 or VAX-11/780. Check SID register for proper jumpering in CPU-type field on backplane.
%BOOT-F-Unexpected exception	Indicates that one of the following exceptions has occurred: Access violation Breakpoint opcode Reserved operand Tbit trap.
%BOOT-F-Unexpected Machine Check	Indicates some sort of machine check occurred. Check all adaptors using console examine and deposit commands. Probably a timeout.

VMB PRIMARY BOOT FAILURE CODES (Cont)

Code	Description
%BOOT-F-Nonexistent Drive	Self explanatory. Check DEFBOO.CMD on 11/750 and make sure system disk is drive being booted.
%BOOT-F-Unable to locate BOOT file	VMB can't find [SYSEXE]SYSBOOT.EXE or if bit 4 in R5 is set, VMB can't find [SYSMAINT]DIAGBOOT.EXE.
%BOOT-F-Bootfile not contiguous	Indicates that [SYSEXE]SYSBOOT.EXE or [SYSMAINT]DIAGBOOT.EXE is not contiguous on system disk. Recopy or rebuild.
%BOOT-F-I/O error reading boot file	Indicates problem reading boot from disk by $QIO service.

SYSTEM CONTROL BLOCK

Vector	Description	Interrupt Priority Level	Interrupt (I) or Exception (E)
SCBB+0	Not used	–	–
SCBB+4	Machine check	1F	E
SCBB+8	Kernel stack invalid	1F	E
SCBB+C	Power fail	1E	I
SCBB+10	Reserved opcode	1F	E
SCBB+14	Customer opcode XFC	1F	E
SCBB+18	Reserved operand	1F	E
SCBB+1C	Reserved address mode	1F	E
SCBB+20	Access violation	1F	E
SCBB+24	Translation invalid	1F	E

SYSTEM CONTROL BLOCK (Cont)

Vector	Description	Interrupt Priority Level	Interrupt (I) or Exception (E)
SCBB+28	Trace trap	1F	E
SCBB+2C	Breakpoint opcode	1F	E
SCBB+30	Compatibility mode	1F	E
SCBB+34	Arithmetic trap	1F	E
SCBB+40	CHMK	1F	E
SCBB+44	CHME	1F	E
SCBB+48	CHMS	1F	E
SCBB+4C	CHMU	1F	E
SCBB+54	Corrected read data	1A	I
SCBB+60	Write bus error	1D	I
SCBB+84	Software interrupt	1	I
SCBB+88	Software interrupt	2	I
SCBB+8C	Software interrupt	3	I
SCBB+90	Software interrupt	4	I
SCBB+94	Software interrupt	5	I
SCBB+98	Software interrupt	6	I
SCBB+9C	Software interrupt	7	I
SCBB+A0	Software interrupt	8	I

SYSTEM CONTROL BLOCK (Cont)

Vector	Description	Interrupt Priority Level	Interrupt (I) or Exception (E)
SCBB+A4	Software interrupt	9	I
SCBB+A8	Software interrupt	A	I
SCBB+AC	Software interrupt	B	I
SCBB+B0	Software interrupt	C	I
SCBB+B4	Software interrupt	D	I
SCBB+B8	Software interrupt	E	I
SCBB+BC	Software interrupt	F	I
SCBB+C0	Interval timer	18	I
SCBB+F0	TU58 receive	14–17	I
SCBB+F4	TU58 transmit	14–17	I
SCBB+F8	Console receive	14	I
SCBB+FC	Console transmit	14	I
SCBB+160	MASSBUS adapter 0	15	I
SCBB+164	MASSBUS adapter 1	15	I
SCBB+168	MASSBUS adapter 2	15	I
SCBB+200	UNIBUS	14–17	I

SPECIAL VECTOR BIT FUNCTIONS

If Vector Bits ⟨1:0⟩ Equal to:	Then:
0	Use kernel stack unless interrupt stack bit in processor status longword is a 1.
1	Use interrupt stack
2	Trap to WCS location 2001, if WCS is not present or disabled, trap to location 0001 in CS. Remove backplane jumper from slot 5 B44 to B48 if WCS is installed.
3	Halt at vector (PC points to interrupted instruction or faulted instruction)

VECTOR MICROADDRESSES

Address	Function	Initiation Method
0000	Power up	–
0011	Arithmetic trap	DO service
0012	FPA integer overflow trap	DO service
0014	Timer service	DO service
0015	T-Bit trap	DO service
0016	Console CTRL/P trap	DO service
0020	Control store parity error	Microtrap
0021	Read unaligned data	Microtrap
0022	MSRC XB Miss	Microtrap
0023	MSRC XB ACV	Microtrap
0024	Write unlock unaligned data	Microtrap
0025	Write unaligned data	Microtrap
0026	Write unlock crossing page boundary	Microtrap

VECTOR MICROADDRESSES (Cont)

Address	Function	Initiation Method
0027	Write crossing page boundary	Microtrap
0028	Machine check exceptions (See note)	Microtrap
0029	But XB Miss	Microtrap
002A	Read TB Miss	Microtrap
002B	Write TB Miss	Microtrap
002C	FPA reserved operand	Microtrap
002D	But XB ACV	Microtrap
002E	Read ACV	Microtrap
002F	Write ACV	Microtrap
0038	Software interrupt	DO service, execution flows
0039	Console interrupt	DO service, execution flows
003A	Unibus interrupt	DO service, execution flows
003B	Interval timer interrupt	DO service, execution flows
003C	Corrected memory interrupt	DO Service, execution flows
003E	Write bus error interrupt	DO service, execution flows

VECTOR MICROADDRESSES (Cont)

Address	Function	Initiation Method
003F	Power fail	DO service, execution flows

NOTE: **MSRC XB TB error**
MSRC XB Bus error
Bus error
Unaligned UNIBUS data
TB error
But XB TB error
But XB Bus error

STACK CONTENTS ON SELECTED VAX EXCEPTIONS

Machine Check

Location	Contents
(SP)	Length parameter
(SP)+4	**Summary parameter code**
(SP)+8	Virtual address
(SP)+C	Program counter
(SP)+10	Memory data register
(SP)+14	Saved mode register
(SP)+18	Read lock time out
(SP)+1C	Translation buffer group register
(SP)+20	Cache error register
(SP)+24	Bus error register
(SP)+28	Memory control error register
(SP)+2C	Program counter
(SP)+30	Processor status longword

Machine Check
Summary Parameter Codes

Code	Description
1	CS parity error
2	Memory error
3	Cache parity error
4	Write bus error
5	Corrected data
7	Bad IRD

Arithmetic Trap

Location	Contents
(SP)	**Error code**
(SP)+4	Program counter
(SP)+8	Program status longword

Arithmetic Trap Error Codes

Code	Description
0	Undefined
1	Integer overflow
2	Integer divide by zero
3	Floating overflow
4	Floating/decimal divide by zero
5	Floating overflow
6	Decimal overflow
7	Subscript out of range

Compatibility Mode

Location	Contents
(SP)	**Error code**
(SP)+4	Program counter
(SP)+8	Program status longword

Compatibility Mode Error Codes

Code	Description
0	PDP-11 reserved operand
1	Breakpoint opcode executed
2	I/O trap
3	Emulator trap
4	Trap
5	Reserved instruction (HALT)
6	Odd address referenced

Translation Not Valid or Access Violation

Location	Contents
(SP)	**Error code**
(SP)+4	Virtual address referenced
(SP)+8	Program counter
(SP)+12	Program status longword

Translation Not Valid or Access Violation Error Codes

Code	Description
0	Read access violation or XB access violation or PTE fetched not valid for read
1	Accessing system 1 space (S1) or length violation
2	No access to process page table (from SPTE)
3	Process PTE VA not in system virtual space
4–7	Same as 0–3 but for write access rather than read access

VAX-11/750 INTERNAL PROCESSOR REGISTERS (IPRS)

Address	Mnemonic	Read Only or Write Only	Name
00	KSP		Kernel stack pointer
01	ESP		Executive stack pointer
02	SSP		Supervisor stack pointer
03	USP		User stack pointer
04	ISP		Interrupt stack pointer
05	Reserved		
06	Reserved		
07	Reserved		
08	P0BR		P0 base register
09	P0LR		P0 length register
0A	P1BR		P1 base register
0B	P1LR		P1 length register
0C	SBR		System base register
0D	SLR		System length register

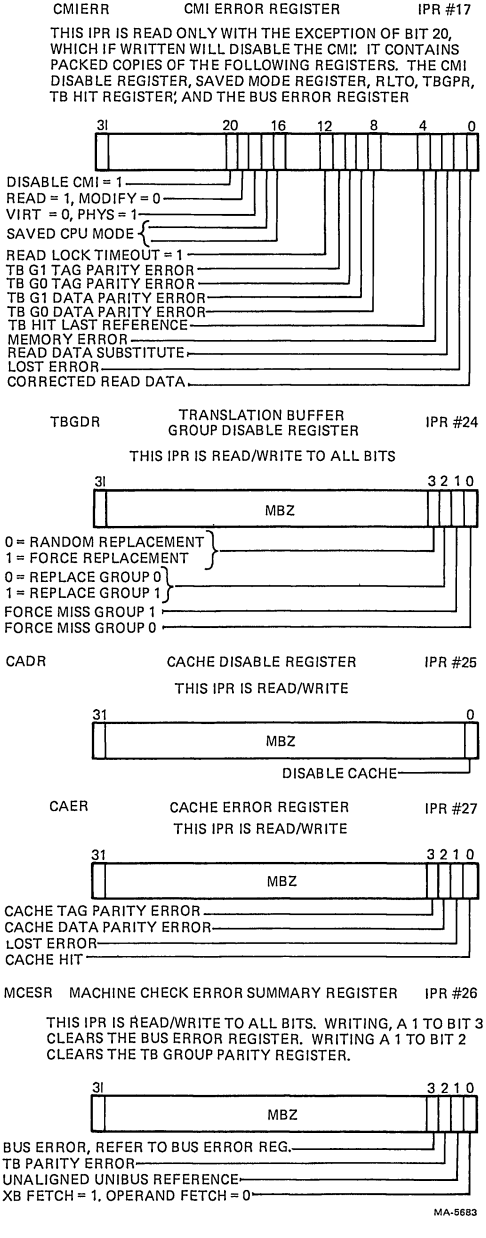

Figure 3 Memory Status and Control Maps

VAX-11/750 INTERNAL PROCESSOR REGISTERS (IPRS) (Cont)

Address	Mnemonic	Read Only or Write Only	Name
0E	Reserved		
0F	Reserved		
10	PCBB		Process control block base
11	SCBB		System control block base
12	IPL		Interrupt priority level
13	ASTR		AST level register
14	SIRR	WO	Software interrupt request register
15	SISR		Software interrupt summary register
16	Reserved		
17	CMIERR	RO	CMI error register
18	ICCS		Interval clock control/status
19	NICR	WO	Next interval count register
1A	ICR	RO	Interval count register
1B	TODR		Time of day register
1C	CSRS		Console storage receiver status
1D	CSRD	RO	Console storage receiver data
1E	CSTS		Console storage transmit status
1F	CSTD	WO	Console storage transmit data

VAX-11/750 INTERNAL PROCESSOR REGISTERS (IPRS) (Cont)

Address	Mnemonic	Read Only or Write Only	Name
20	RXCS		Console receive control/status
21	RXDB	RO	Console receive data buffer
22	TXCS		Console transmit control/status
23	TXDB	WO	Console transmit data buffer
24	TBDR		Translation buffer disable register
25	CADR		Cache disable register
26	MCESR		Machine check error summary register
27	CAER		Cache error register
28	ACCS	RO	Accelerator control/ status register
29	Reserved		
2A	Reserved		
2B	Reserved		
2C	Reserved		
2D	Reserved		
2E	Reserved		
2F	Reserved		
30	Reserved		
31	Reserved		
32	Reserved		
33	Reserved		

VAX-11/750 INTERNAL PROCESSOR REGISTERS (IPRS) (Cont)

Address	Mnemonic	Read Only or Write Only	Name
34	Reserved		
35	Reserved		
36	Reserved		
37	IO RESET	WO	Initialize UNIBUS
38	MME		Memory management enable
39	TBIA	WO	Translation buffer invalidate all
3A	TBIS	WO	Translation buffer invalidate single
3B	TB DATA		Translation buffer data
3C	Reserved		
3D	PMR		Performance monitor register
3E	SID	RO	System identification
3F	Reserved		

BLANK

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